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Optimization design of microchannel cooling heat sink

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Abstract

Purpose – This paper sets out to optimize the shape and size of microchannels cooling heat sink, which has been widely used to cool electronic chip for its high heat transfer coefficient and compact structure.

Design/methodology/approach – Sequential Quadratic Programming (SQP) method is used to optimize the cross-section sizes of microchannels. Finite volume method is used to numerically simulate the cooling performance of optimal microchannel cooling heat sink.

Findings – The optimized cross-section shape of microchannel is rectangular, and the width and depth of microchannel is 50 and 1,000 μm, respectively, the number of microchannels is 60, and the corresponding least thermal resistance is 0.115996°C/W. The results show that the heat transfer performance of microchannel cooling heat sink is affected intensively by its cross-section shape and dimension. The convection heat resistance R_{conv} between inner surface in microchannels and working fluid has more influence in the total heat resistance. The heat flux of chip is 278 W/cm^2 and, through the optimization microchannel cooling heat sink, the highest temperature in the chip can be kept below 42°C, which is about half of that without optimizing heat sink and can ensure the stability and reliability of chip.

Research limitations/implications – The convection heat transfer coefficient is calculated approximatively here for convenience, and that may induce some errors.

Originality/value – The optimized microchannels cooling heat sink may satisfy the request for removal of high heat flux in new-generation chips.

Keywords Optimization techniques, Heat transfer, MEMS

Paper type Research paper

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1. Introduction

With the developments of world spaceflight science and technology, Micro-electromechanical Systems (MEMS), and micro-machining technology, micro-satellite has rapidly been developed for its low cost, light weight, short period, high function density, and flexible launch. While the dimension, volume and mass of satellite is decreasing, its function does not change or even become more powerful, which leads to higher heat transferred in micro space and time. Cumulating heat will result in the rise of temperature of devices, while the reliability of micro-electronics components and devices is sensitive to temperature. When the device temperature increases 1°C above 70 ~ 80°C, the reliability decreases 5 percent (Zengyuan, 1988). The major heat resource in micro-electronic devices is chip, and what kind of cooling method can be used to keep the stable and reliable operation of the devices is present primary problem to be solved in micro-electronic industry.

When the heat flux of micro-electronic devices exceeds 100 W/cm^2, traditional cooling method by air is unlikely to meet the cooling needs, and other means of thermal management have to be considered. Among those, microchannel cooling heat sink has emerged as one of the effective cooling techniques, apparently first proposed by Tuckerman and Pease (Kleiner *et al.*, 1995) to cool electronic devices. They built a water-cooled integral heat sink with microscopic flow channels, and demonstrated that extremely high-power density with a heat flux as high as 790 W/cm^2 could be dissipated. Peng and Peterson (1996) performed experimental investigations on the pressure drop and convective heat transfer for water flow in rectangular microchannels, and found that the cross sectional aspect ratio had great influence on the flow friction and convective heat transfer both in laminar and turbulent flows. A numerical simulation of forced convection heat transfer occurring in silicon-based microchannels heat sinks has been conducted by Li *et al.* (2004) using a simplified 3D conjugate heat transfer model (2D fluid flow and 3D heat transfer). The results indicate that thermophysical properties of the liquid can significantly influence both the flow and heat transfer in the microchannel heat sink. Lee *et al.* (2005) experimentally investigated the validity of classical correlations based on conventional sized channels for predicting the thermal behavior in single-phase flow through rectangular microchannels. Numerical predictions obtained based on a classical, continuum approach were found to be in good agreement with the experimental data, suggesting that a conventional analysis approach can be employed in predicting heat transfer behavior in microchannels of the dimensions considered in that study. Harms *et al.* (1999) experimentally investigated the single-phase forced convection in deep rectangular microchannels. The experimentally obtained local Nusselt number agrees reasonably well with classical developing channel flow theory. Morini (2004) reviewed the convective heat transfer through microchannels, and compared the experimental results quoted in the open literature. Rarefaction and compressibility effects, viscous dissipation effects, electro-osmotic effects, property variation effects, channel surface conditions (relative roughness) and experimental uncertainties have been invoked to explain the anomalous behavior of the transport mechanisms through microchannels. All open literatures show that there was difference between some experimental results and conventional prediction results by classical theory, and different authors have different experimental results. Therefore, the problem needed to be resolved is what method is used to design a kind of microchannel heat sink with high heat transfer performance and least thermal resistance, which is investigated in this paper.

2. Optimization of microchannel cooling heat sink

In the design of microchannel cooling heat sink, the silicon-based microchannels are directly etched on back of chip for high thermal conductivity of silicon and to decrease the contact thermal resistance between the chip and microchannels. The structural dimension of microchannels for least thermal resistance can be attained by optimization design. Sasaki and Kishimoto (1986) optimal the channel dimensions of a finned heat sink constructed on a silicon chip for a given pressure drop. The ratio of width of channel and fin was restricted to unity, and the optimal channel widths were found to be 400 and 250 μm for a pressure drop of 200 and 2,000 kg/m^2, respectively. Ryu *et al.* (2003) adopted an optimization scheme based on the steepest descent method to optimize a manifold microchannels heat sink. For given pumping power, the optimal design variables that minimize the thermal resistance are obtained iteratively. Among various design variables, the channel width and depth are more crucial than others to the heat-sink performance. The optimal microchannel width and depth are 16 and 140 μm, respectively, and the corresponding thermal resistance is 0.031°C/W. Otherwise, they (Ryu *et al.*, 2002) optimized the monolayer microchannels heat sink. The optimal results are: microchannel number, width, depth, and substrate thickness are 124, 45.3, 100, and 453 μm, respectively, and corresponding thermal resistance 0.069°C/W. The optimization results have relation with given pumping power. Because the dimensions of microchannels are small, if manifold microchannels are used, in which the volume of fluid will be less, and heat transfer through fluid flow will decrease, too. So monolayer microchannels are designed by optimization method in this paper. The monolayer microchannels are shown in Figure 1, when $w_{c1} = w_{c2}$, the microchannel is rectangle, when $w_{c2} = 0$, the microchannel is triangular, else the microchannel is trapezoidal form.

3. Optimization design problem

Heat transfer performance of microchannel cooling heat sink is characterized by the total heat resistance (Birur *et al.*, 2001), defined by:

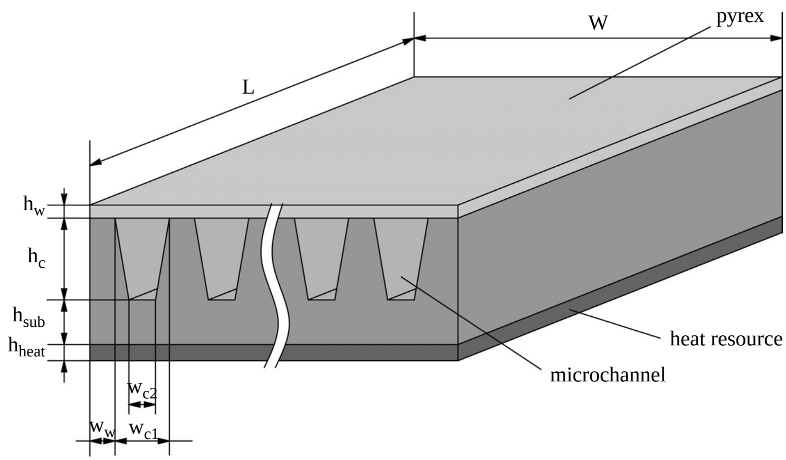

Figure 1.
Schematic diagram of monolayer microchannels heat sink

$$R_{total} = \frac{(T_{heater} - T_{in})}{q} \tag{1}$$

where T_{heater} is the temperature of chip, T_{in} is the bulk temperature of inlet fluid, and q is the power of heat resource. The effect of viscous heating is negligible in analysis. The total thermal resistance has three main components:

(1) conductive resistance through the substrate between the chip surface and the microchannel base plane, R_{cond} (because the thermal conductivity of substrate is large and the microchannels are fabricated directly in the substrate, the conductive resistance is small and can be neglected, as shown in Knight *et al.* (1992));

(2) convective resistance from the microchannel surface to the working fluid, R_{conv}; and

(3) temperature rise resistance from the bulk temperature rise of the working fluid from the inlet, R_{heat}, and the corresponding expression is expressed as:

$$R_{total} = R_{cond} + R_{conv} + R_{heat} = \frac{h_{sub}}{k_s A_h} + \frac{1}{n h_{conv} A_c} + \frac{1}{\dot{m} c_p} \tag{2}$$

where h_{sub} is the distance from the chip surface to the base of the microchannels, k_s is the thermal conductivity of the substrate, A_h is the bottom area of the microchannel, n is the number of microchannels, h_{conv} is the convective heat transfer coefficient, A_c is the wetted area, $\dot{m}$ is the mass flow rate and c_p is the specific heat of the working fluid:

$$A_h = L(n w_{c1} + (n+1) w_w), \quad A_c = L\left(w_{c2} + 2\eta_f \sqrt{h_c^2 + \left(\frac{w_{c1} - w_{c2}}{2}\right)^2}\right), \tag{3}$$

$$\dot{m} = \rho_f Q$$

where w_{c1} is the top width of microchannel, w_{c2} is the bottom width of microchannel, h_c is the depth of microchannel, w_w is the width of fin, η_f is the wetted coefficient, Q is volume flow rate of working fluid, and ρ_f is density of working fluid. In addition, all thermophysical properties are assumed constant.

The convection heat transfer coefficient h_{conv} is related with geometry and dimensions of microchannel and the velocity, thermophysical properties of working fluid, and is a complex function of Prandtl number and Nusselt number. For convenience here, the convection heat transfer coefficient is calculated approximatively. If the dimension of chip is $L \times W = 6 \times 6$ mm, and the power is 100 W, and the largest temperature difference between wall and fluid is 100°C, the convection heat transfer coefficient is about 28,000 W/m^2°C.

Suppose the density of working fluid is $\rho_f = 1{,}000\,\text{kg/m}^3$, the specific heat is $c_p = 4{,}179$ J/kg°C, the distance from the chip surface to the base of the microchannels h_{sub} is 100 μm, the thermal conductivity of the substrate is $k_s = 353.356$ W/m°C, and the dimension of chip is $L \times W = 6 \times 6$ mm. If the fluid flow in microchannels is fully developed, the wetted coefficient $\eta_f = 1$. Select the number of microchannel n, the top width of microchannel w_{c1}, the width of fin w_w, the depth of microchannel h_c, and the bottom width of microchannel w_{c2} as design variable, expressed as x_1, x_2, x_3, x_4, and x_5.

When the pumping power is given 0.443 W, the corresponding volume flow rate of working fluid is about $4 \times 10^{-6}\,\mathrm{m^3/s}$. Considering the fabrication difficulty, the bottom width of microchannel is less than the top width, and the width of channel and fin is larger than 50 nm. Select the total thermal resistance R_{total} as objective function and the problem can be translated into the constrained non-linear programming optimization problem:

$$\begin{cases} \text{Find} & x_1, x_2, x_3, x_4, x_5 \\ \min & f(x_1,x_2,x_3) = \frac{4.717\times 10^{-5}}{x_1x_2+(x_1+1)x_3} + \frac{0.00595}{x_1\left(x_5+2\sqrt{x_4^2+\left(\frac{x_2-x_5}{2}\right)^2}\right)} + 0.059825 \\ \text{s.t.} & x_1x_2+(x_1+1)x_3 - 0.006 = 0 \\ & x_5 - x_2 \le 0 \\ & 10 \le x_1 \le 300 \\ & 5\times 10^{-5} \le x_2 \le 1\times 10^{-3} \\ & 5\times 10^{-6} \le x_3 \le 1\times 10^{-3} \\ & 5\times 10^{-5} \le x_4 \le 1\times 10^{-3} \\ & 0 \le x_5 \le 1\times 10^{-3} \end{cases} \tag{4}$$

4. Optimization design method

Sequential Quadratic Programming (SQP) method is used to optimize the above problem. The SQP implementation consists of three main stages: updating of the Hessian matrix of the Lagrangian function, quadratic programming problem solution, and line search and merit function calculation.

4.1 Updating the Hessian matrix

At each major iteration a positive definite *quasi*-Newton approximation of the Hessian of the Lagrangian function, H, is calculated using the BFGS method, where $\lambda_i (i = 1, \ldots, m)$ is an estimate of the Lagrange multipliers:

$$H_{k+1} = H_k + \frac{q_k q_k^T}{q_k^T s_k} - \frac{H_k^T H_k}{s_k^T H_k s_k} \tag{5}$$

where $s_k = x_{k+1} - x_k$:

$$q_k = \nabla f(x_{k+1}) + \sum_{i=1}^{n} \lambda_i \cdot \nabla g_i(x_{k+1}) - \left(\nabla f(x_k) + \sum_{i=1}^{n} \lambda_i \cdot \nabla g_i(x_k)\right)$$

4.2 Quadratic programming solution

At each major iteration of the SQP method, a QP problem of the following form is solved, where A_i refers to the ith row of the m-by-n matrix $\mathbf{A}$:

$$\begin{aligned} &\underset{d\in\Re^n}{\text{minimize}} \quad q(d) = \tfrac{1}{2}\, d^{\mathrm{T}}Hd + c^{\mathrm{T}}d \\ &A_i d = b_i \qquad i = 1, \ldots, m_e \\ &A_i d \le b_i \qquad i = m_e + 1, \ldots, m \end{aligned} \tag{6}$$

The solution procedure involves two phases. The first phase involves the calculation of a feasible point (if one exists). The second phase involves the generation of an iterative sequence of feasible points that converge to the solution.

4.3 Line search and merit function

The solution to the QP subproblem produces a vector $\mathbf{d}_k$, which is used to form a new iterate:

$$x_{k+1} = x_k + \alpha\mathbf{d}_k \tag{7}$$

The step length parameter α is determined in order to produce a sufficient decrease in a merit function. The merit function of the following form is used in this implementation:

$$\Psi(x) = f(x) + \sum_{i=1}^{m_e} r_i \cdot g_i(x) + \sum_{i=m_e+1}^{m} r_i \quad \max\{0, g_i(x)\} \tag{8}$$

The penalty parameter is set to:

$$r_i = (r_{k+1})_i = \max_i \left\{\lambda_i, \frac{1}{2}((r_k)_i + \lambda_i)\right\}, \quad i = 1, \ldots, m \tag{9}$$

This allows positive contribution from constraints that are inactive in the QP solution but were recently active. In this implementation, the penalty parameter r_i is initially set to:

$$r_i = \frac{|\nabla f(x)|}{|\nabla g_i(x)|} \tag{10}$$

where | | represents the Euclidean norm.

This ensures larger contributions to the penalty parameter from constraints with smaller gradients, which would be the case for active constraints at the solution point.

5. Optimization results and discussion

Initial value does not affect optimization results significantly, but suitable initial value can decrease iteration time. The initial value is chosen as $x0 = [10, 5\times10^{-4}, 8\times10^{-4}, 5\times10^{-4}, 5\times10^{-4}]$ in this paper, and the total thermal resistance is converged to 0.115996°C/W after 12 iterations. The iteration history of total thermal resistance is shown in Figure 2, and optimal design variables are listed in Table I.

Optimal results of shape dimensions of microchannel cooling heat sink in Table I show that when the microchannel shape is rectangle, the corresponding thermal resistance is least, and the heat transfer performance of microchannel cooling heat sink is best. The main reason may be the contact area between working fluid and microchannels and the bottom area of the microchannel is largest for rectangle simultaneously.

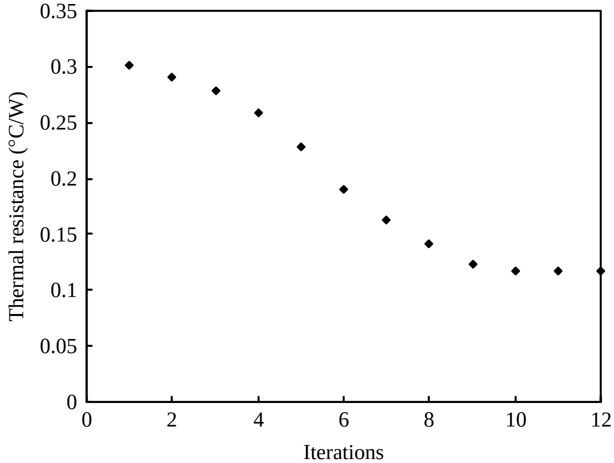

Figure 2.
Total thermal resistance varies with iteration number

W_{c1} (μm)	W_{c2} (μm)	N	h_c (μm)	w_w (μm)	h_{sub} (μm)
50	50	60	1,000	50	100

Table I.
Note: Shape dimensions of optimal microchannel cooling heat sink

The total and component thermal resistances are listed in Table II, which show that the convective thermal resistance R_{conv} and temperature rise resistance R_{heat} are larger than conductive thermal resistance. Since, microchannels are fabricated directly in the chip, which eliminate the thermal contact resistance between microchannel cooling heat sink and chip, and the substrate thickness is usually small and the thermal conductivity of silicon is large, R_{cond} is usually very small and for most practical purposes can be neglected. The reason that convective thermal resistance R_{conv} is less than temperature rise resistance R_{heat}, which is different from the conclusion of Birur *et al.* (2001), is the pumping power is very low in this study, result in a comparatively high temperature rise resistance R_{heat}.

The result of total thermal resistance in this paper is larger than that of Ryu *et al.* (2002). The main reason is the pumping power is constrained in a small value (about 0.443 W), which results in a less volume flow rate. In addition, the dimension of whole microchannel heat sink is less, so the total thermal resistance is larger, but it still can satisfy the need of cooling high power chip.

The numerical simulation is used to verify the cooling performance of optimal microchannel cooling heat sink by using electronics cooling software (Icepak Reference Manual, 1999) that has been previously used in analyzing the heat transfer character in

R_{total} (°C/W)	R_{cond} (°C/W)	R_{conv} (°C/W)	R_{heat} (°C/W)
0.115996	0.007797	0.048374	0.059825

Table II.
Note: Optimization results of total and component thermal resistance

electronics and chip cooling applications, which uses finite volume method to solve computational fluid dynamics problem. The dimension of chip is $L \times W = 6 \times 6$ mm, and the power is 100 W, the corresponding heat flux is 278 W/cm^2. The inlet temperature of working fluid is 20°C, the volume flow rate is 4×10^{-6} m^3/s, inlet pressure is 1.0135×10^5 N/m^2, and outlet pressure is 0 N/m^2. The corresponding Reynolds Number is 127, therefore the flow is laminar. To compare with microchannel cooling heat sink without optimizing, another heat sink is simulated too. The microchannel number of the heat sink is 20, and the width of microchannel is 250 μm, and the corresponding Reynolds Number is 320. The simulation results are shown in Figures 3 and 4, which show that the highest temperature of heat sink before optimizing is 80.5040°C, while the highest temperature of optimal microchannel heat sink is 41.8402°C. The optimal heat sink can completely satisfy the need of high power chip for stability and reliability.

6. Conclusion

For the higher heat transfer coefficient and compact structure, microchannel cooling heat sink has widely been used to cool electronic chip currently and in the future. According the characteristic of micro-satellite restricted to small structure dimensions, the heat transfer performance of a novel method to cool microchip – microchannel cooling heat sink is investigated in this paper. SQP method is used to optimize the shape and dimensions of the microchannel, and the effect of the dimensions of the microchannel cross section on the heat transfer performance is analyzed. Some conclusions are drawn:

(1) The total thermal resistance has three main components:
   - conductive resistance through the substrate between the chip surface and the microchannel base plane, R_{cond};

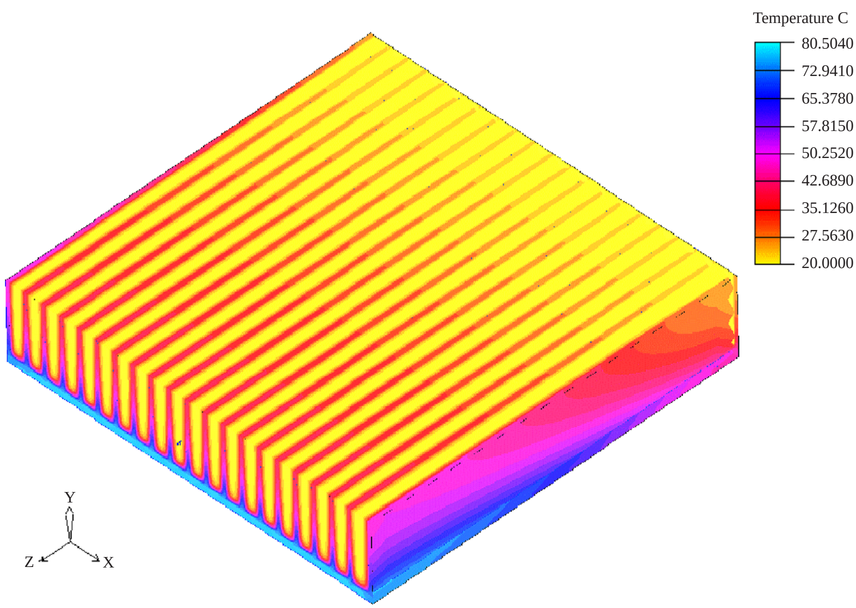

Figure 3. Numerical simulation results of microchannel cooling heat sink before optimizing

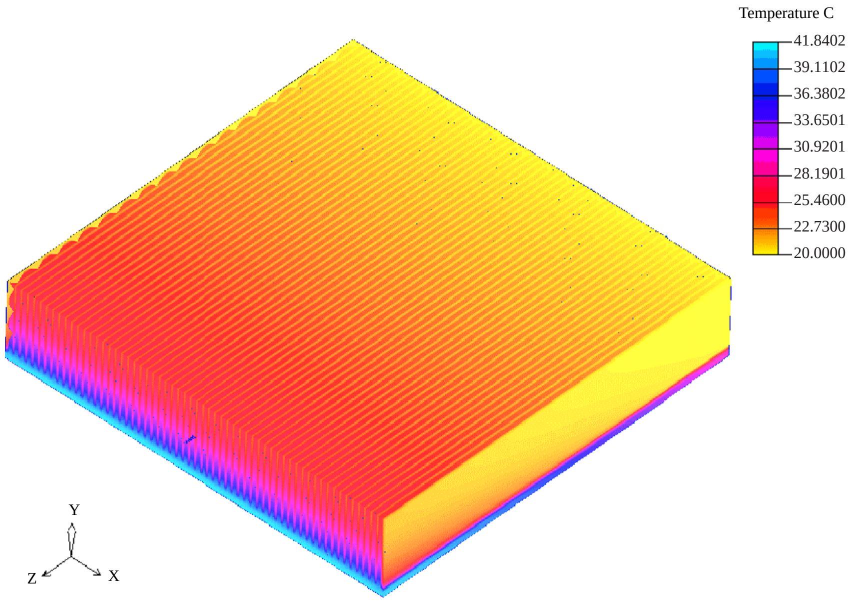

Figure 4.
Numerical simulation results of optimal microchannel cooling heat sink

- convective resistance from the microchannel surface to the working fluid, R_{conv}; and
- temperature rise resistance from the bulk temperature rise of the working fluid from the device inlet, R_{heat}.

The calculation results show that the convective thermal resistance R_{conv} and temperature rise resistance R_{heat} are larger than conductive thermal resistance, so the conductive resistance can be neglected usually.

(2) Because the thermal conductivity of working fluid is far less than that of silicon-based microchannel, narrow microchannel has more contact area between fluid and heat sink, which can absorb more heat through fins. However, because of difficulty of fabrication on the one hand, and enough fluid has to be flowed in microchannel to transfer heat produced by chip on the other hand, the width of microchannel cannot be too small. The optimal width of microchannel is 50 μm, which is the least limit of fabrication, and the corresponding least thermal resistance is 0.115996°C/W.

(3) Though high-volume rate can transfer more heat by working fluid, but the pumping power is increased simultaneously. In the design of micro-satellite, the energy cost of system is constrained. Limited by the pumping power, the volume rate of working fluid is low, which result in the thermal resistance obtained in this paper is larger than that of Ryu *et al.* (2002). However, the need to cool high power chip can still be satisfied.

(4) Finite volume method is used to numerically simulate the cooling performance of optimal microchannel cooling heat sink. The heat flux of chip is 278 W/cm^2 and through the optimal microchannel heat sink, the highest temperature can be

kept below 42°C, which is about half of that of without optimizing heat sink, and can ensure the stability and reliability of chip.

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Further reading

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